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☐	L5	L4 not L3	266
☐	L4	L2 and (implant$4 with mask$3)	272
☐	L3	L2 and titanium and (tantalum adj nitride)	91
☐	L2	L1 and (overlap$4 with gate)	707
☐	L1	438/149,151,163,164,166,197,299,301.ccls.	3985

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		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L2	TFT and (gate with first with conduct$4) and (gate with second with conduct$4) and (etch$3 with select$5) and (overlap$5 with gate)	1017
☐	L1	TFT and (titanium) and (tantalum adj nitride) and (SF6 or (sulfur adj hexafluoride))	7

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☐	L7	L6 and (etch$4 with (taper$4 or angl$4 or inclin$6))	511
☐	L6	L4 or L5	984
☐	L5	L3 and inclin$7	86
☐	L4	L3 and (taper$4 or angl$4)	968
☐	L3	L2 and LDD	1425
☐	L2	L1 and (titanium or Ti)	2394
☐	L1	(gate with overlap$5) and ((hot adj carrier$1) or (drain with field))	6518

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DB=PGPB,USPT; PLUR=YES; OP=OR			
L13	6706544.pn. and titanium	1	L13
L12	6596571.pn.	1	L12
L11	6933184.pn.	1	L11
L10	L9 and (ion$1 or implant$5)	3	L10
L9	L8 and etch$5	3	L9
L8	L1 and (titanium and (tantalum adj nitride))	3	L8
L7	L5 and SF6	1	L7
L6	L5 and (sulfur adj hexafluoride)	0	L6
L5	L4 and (selectiv$5 with etch$6)	7	L5
L4	L3 and (titanium and (tantalum adj nitride))	7	L4
L3	L1 or L2	11	L3
DB=PGPB; PLUR=YES; OP=OR			
	(20040140472 or 20030100151 or 20030062524 or 20030020118 or		

L2	20020163049 or 20020000576 or 20010055841 or 20010048408).pn.	8	L2
DB=USPT; PLUR=YES; OP=OR			
L1	(6706544 or 6933184 or 6872604).pn.	3	L1

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		DB=USPT; PLUR=YES; OP=OR	
☐	L2	L1 and (overlap$4 or taper$4).clm.	35
☐	L1	438/163.ccls.	288

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1. **Analysis of electrical characteristics of gate overlapped lightly doped drain (GOLDD) polysil transistors with different LDD doping concentration**
Bonfiglietti, A.; Cuscuna, M.; Valletta, A.; Mariucci, L.; Pecora, A.; Fortunato, G.; Brotherton, S.D.; A
Electron Devices, IEEE Transactions on
Volume 50, Issue 12, Dec. 2003 Page(s):2425 - 2433
Digital Object Identifier 10.1109/TED.2003.819250
AbstractPlus | References | Full Text: PDF(672 KB) IEEE JNL

2. **Improved lifetime of poly-Si TFTs with a self-aligned gate-overlapped LDD structure**
Mishima, Y.; Ebiko, Y.;
Electron Devices, IEEE Transactions on
Volume 49, Issue 6, June 2002 Page(s):981 - 985
Digital Object Identifier 10.1109/TED.2002.1003716
AbstractPlus | References | Full Text: PDF(234 KB) IEEE JNL

3. **Hot carrier-induced degradation of gate overlapped lightly doped drain (GOLDD) polysilicon**
Valletta, A.; Mariucci, L.; Fortunato, G.; Brotherton, S.D.; Ayres, J.R.;
Electron Devices, IEEE Transactions on
Volume 49, Issue 4, April 2002 Page(s):636 - 642
Digital Object Identifier 10.1109/16.992873
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4. **A new dopant activation technique for poly-Si TFTs with a self-aligned gate-overlapped LDD**
Ohgata, K.; Mishima, Y.; Sasaki, N.;
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10-13 Dec. 2000 Page(s):205 - 208
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5. **A high speed and high reliability MOSFET utilizing an auxiliary gate**
Minami, M.; Sawahata, Y.; Matsuki, H.; Nagano, T.;
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4-7 June 1990 Page(s):41 - 42
Digital Object Identifier 10.1109/VLSIT.1990.110998
AbstractPlus | Full Text: PDF(124 KB) IEEE CNF

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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

1. **Gated-four-probe a-SI:H thin-film transistor structure**
Chun-Ying Chen; Chun-Sung Chiang; Kanicki, J.;
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23-25 June 1997 Page(s):52 - 53
Digital Object Identifier 10.1109/DRC.1997.612471
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2. **Gate-overlapped lightly doped drain poly-SI thin-film transistors for large area-AMLCD**
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8. **Flicker noise in gate overlapped polycrystalline silicon thin-film transistors**
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